FPD2250DFN

LOW NOISE, HIGH LINEARITY PACKAGED PHEMTT

- PERFORMANCE (1850 MHz)
  - 29 dBm Output Power (P_{1dB})
  - 16.5 dB Small-Signal Gain (SSG)
  - 1.0 dB Noise Figure
  - 42 dBm Output IP3
  - 50% Power-Added Efficiency
  - Evaluation Boards Available
  - Featuring Lead Free Finish Package

- DESCRIPTION AND APPLICATIONS

The FPD2250DFN is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 μm x 1500 μm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and input power levels. The FPD2250DFN is available in die form and in other packages.

Typical applications include drivers or output stages in PCS/Cellular base station high-intercept-point LNAs, WLL and WLAN systems, and other types of wireless infrastructure systems.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT *f* = 1850 MHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}	28	29		dBm
Small-Signal Gain	SSG	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}	15	16.5		dB
Power-Added Efficiency	PAE	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}; P_{OUT} = P_{1dB}		50		%
Noise Figure	NF	V_{DS} = 5 V; I_{DS} = 50% I_{DSS}		1.0	1.75	dB
		V_{DS} = 5 V; I_{DS} = 25% I_{DSS}		0.8		
Output Third-Order Intercept Point (from 15 to 5 dB below P_{1dB})	IP3	V_{DS} = 5V; I_{DS} = 50% I_{DSS}				
		Matched for optimal power		42		dBm
		Matched for best IP3		43		
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	560	700	825	mA
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		1.1		A
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		600		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -5 V		1	10	μA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 2.25 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 2.25 mA	12	16		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 2.25 mA	12	16		V

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		8	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward or reverse current		22	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		525	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		3.0	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1] $T_{Ambient}$ = 22°C unless otherwise noted [2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1

[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where:

  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Total Power Dissipation to be de-rated as follows above 22°C:

  P_{TOT}= 3.0W – (0.025W/°C) x T_{PACK}
  where T_{PACK} = *package lead temperature above 22°C*
  (coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 65°C package lead temperature: P_{TOT} = 3.0W – (0.025 x (65 – 22)) = 1.93W

- **The use of a filled via-hole directly beneath the exposed heatsink tab on the bottom of the package is strongly recommended to provide for adequate thermal management. Ideally the bottom of the circuit board is affixed to a heatsink or thermal radiator.**

HANDLING PRECAUTIONS

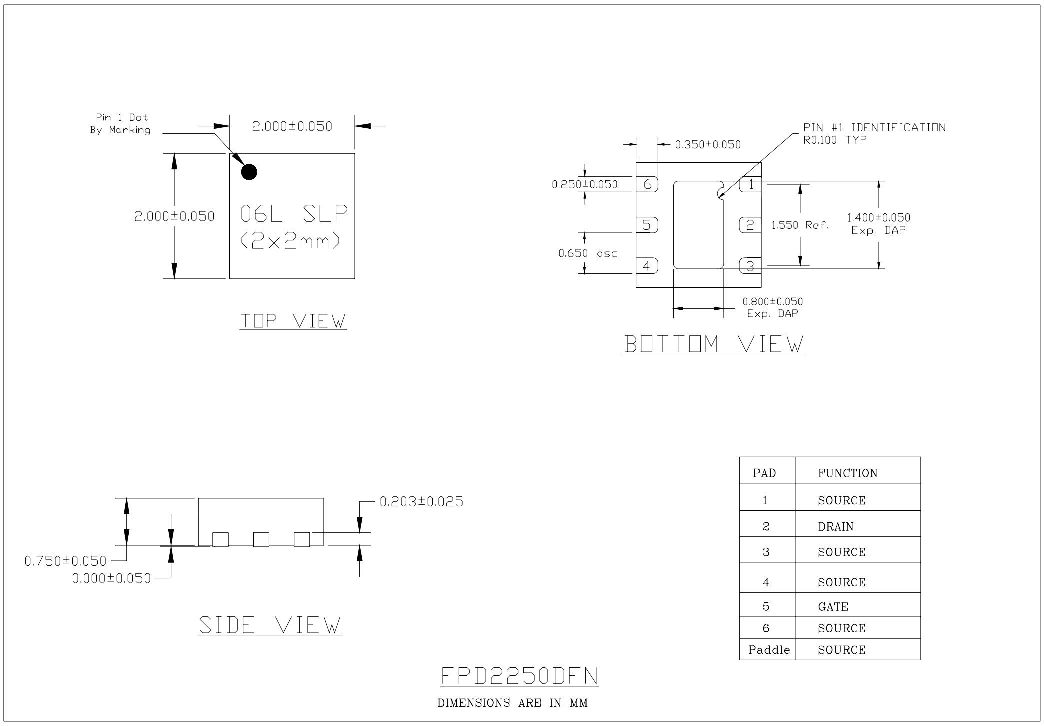
To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site. Evaluation Boards available upon request.

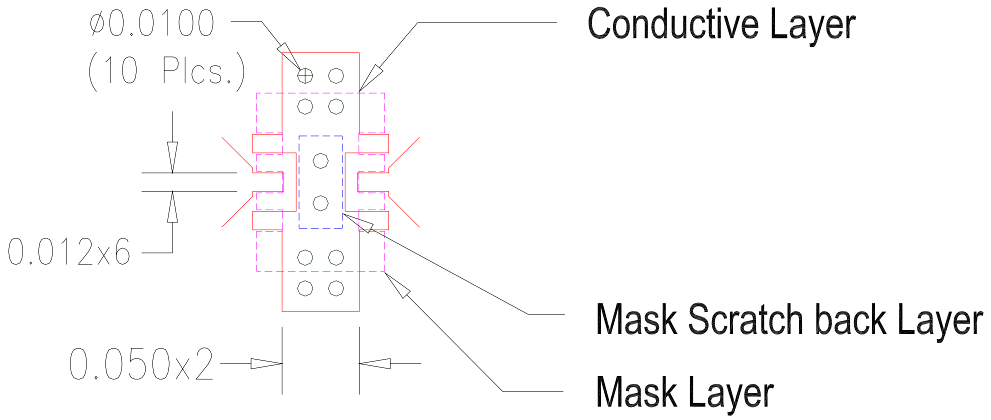
- BIASING GUIDELINES
  - Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
  - Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD2250DFN.
  - For standard Class A operation, a 50% of I_{DSS} bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are "quasi- E/D mode" devices, exhibit Class AB traits when operated at 50% of I_{DSS}. To achieve a larger separation between P_{1dB} and IP3, an operating point in the 25% to 33% of I_{DSS} range is suggested. Such Class AB operation will not degrade the IP3 performance.

- PACKAGE OUTLINE (dimensions in mm)



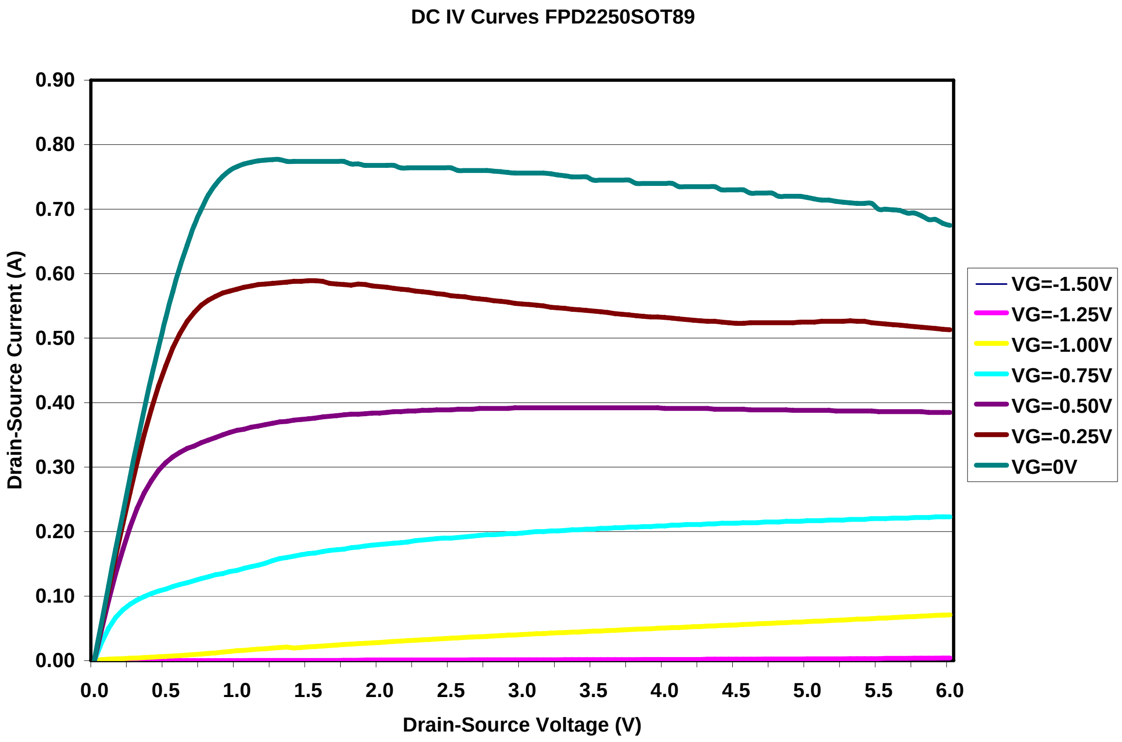
PAD	FUNCTION
1	SOURCE
2	DRAIN
3	SOURCE
4	SOURCE
5	GATE
6	SOURCE
Paddle	SOURCE

- PCB FOOT PRINT



Dimensions are in Inches

- TYPICAL I-V CHARACTERISTICS



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the $V_{DS} > 1.3V$ will generally cause errors in the current measurements, even in stabilized circuits.

Recommendation: Traditionally a device's I_{DSS} rating (I_{DS} at $V_{GS} = 0V$) was used as a predictor of RF power, and for MESFETs there is a correlation between I_{DSS} and P_{1dB} (power at 1dB gain compression). For pHEMTs it can be shown that there is *no* meaningful statistical correlation between I_{DSS} and P_{1dB}; specifically a linear regression analysis shows $r^2 < 0.7$, and the regression fails the F-statistic test. I_{DSS} is sometimes useful as a guide to circuit tuning, since the S_{22} does vary with the quiescent operating point I_{DS}.